

Fig. 1

NODE  
INTERCONNECT

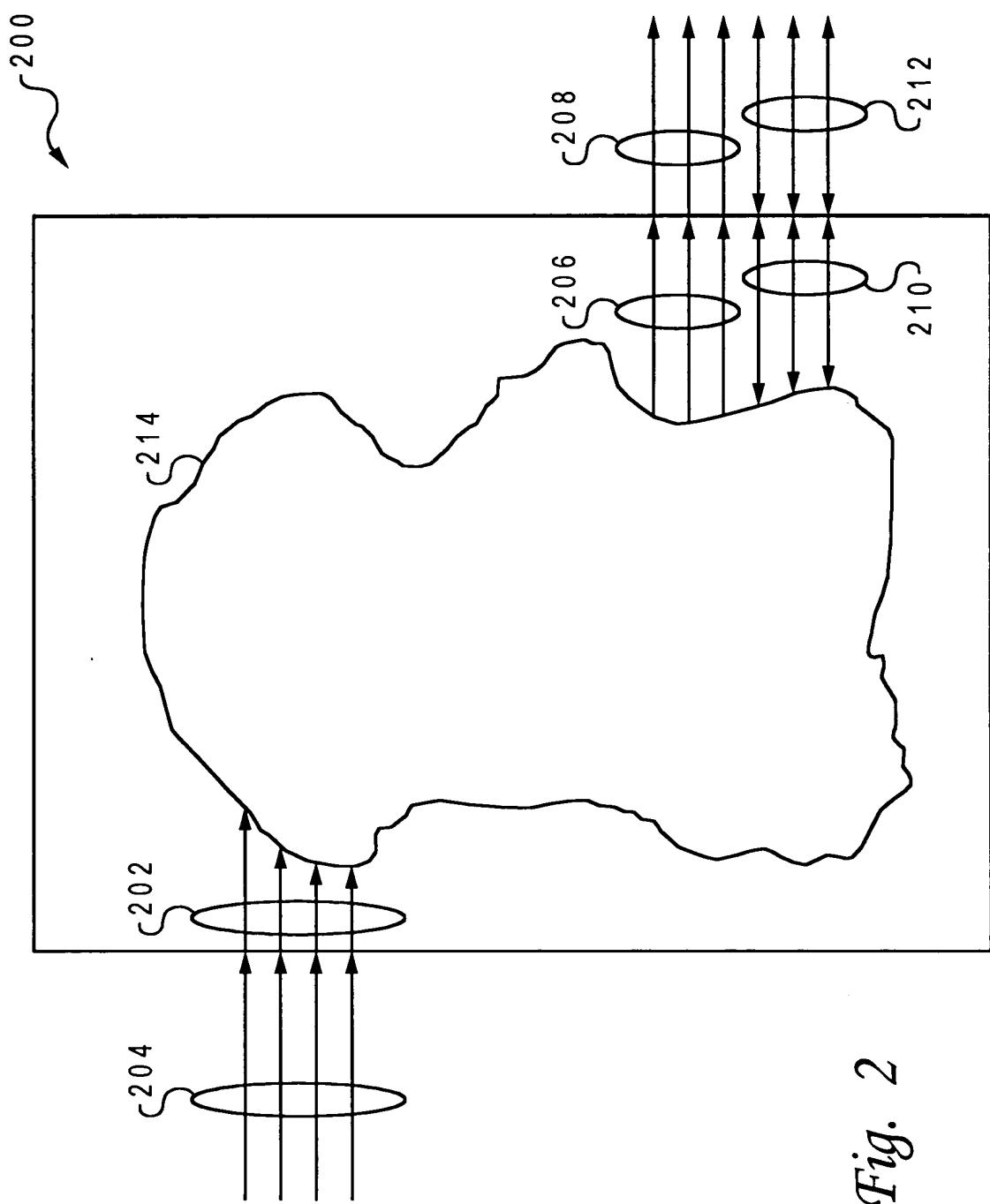


Fig. 2

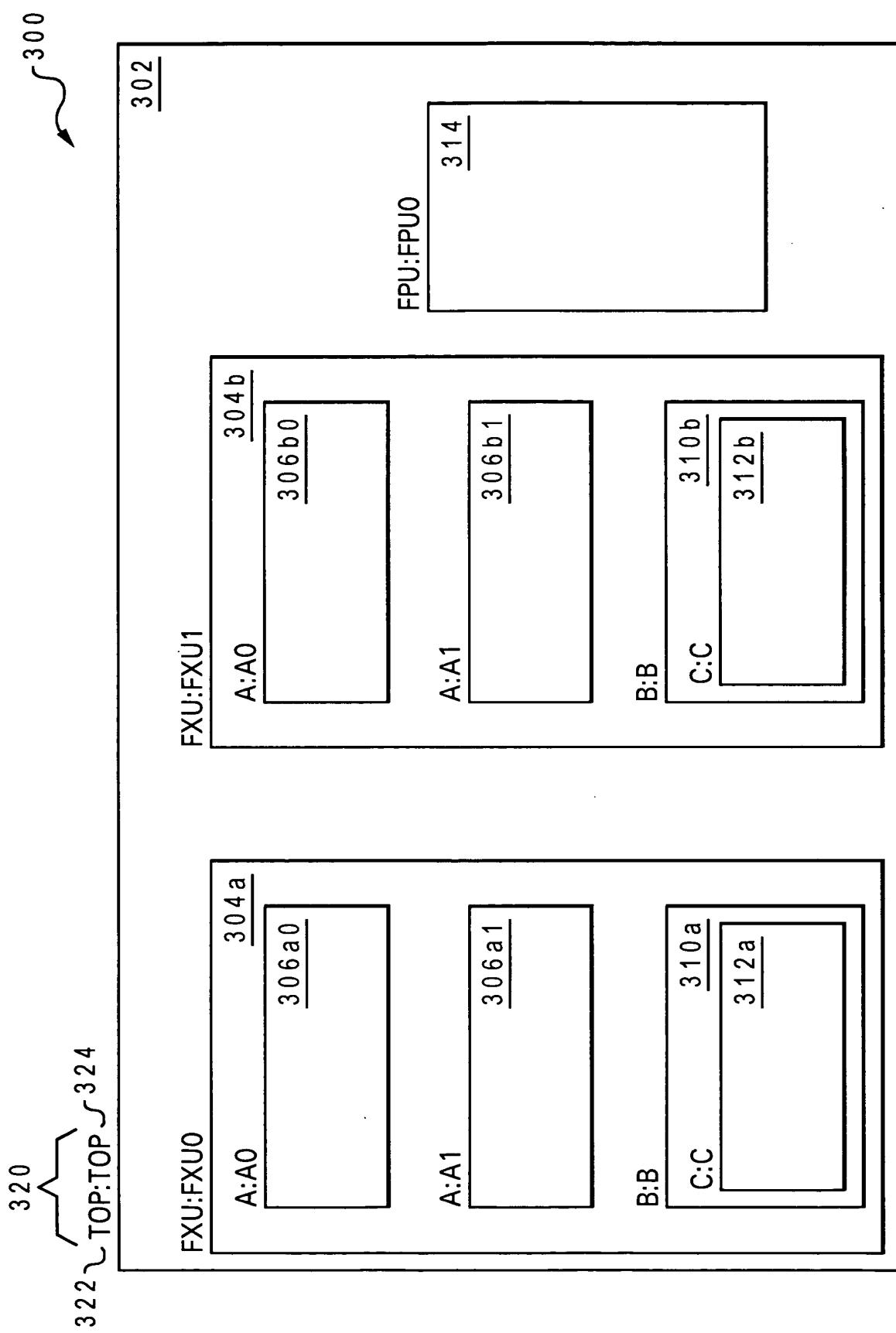


Fig. 3

400

```
ENTITY A IS
  PORT
  (
    ...
    );
  END A;

  ARCHITECTURE A OF A IS
  ...
  BEGIN
    ...
    --## statementA
    --## statementB
    --## statementC
    ...
    --## statementD
    --## statementE
    --## statementF
    ...
  END;
```

402      -- port\_list

404      -- signal declarations

406      -- HDL code describing design

408      -- HDL code describing design

410

*Fig. 4A*

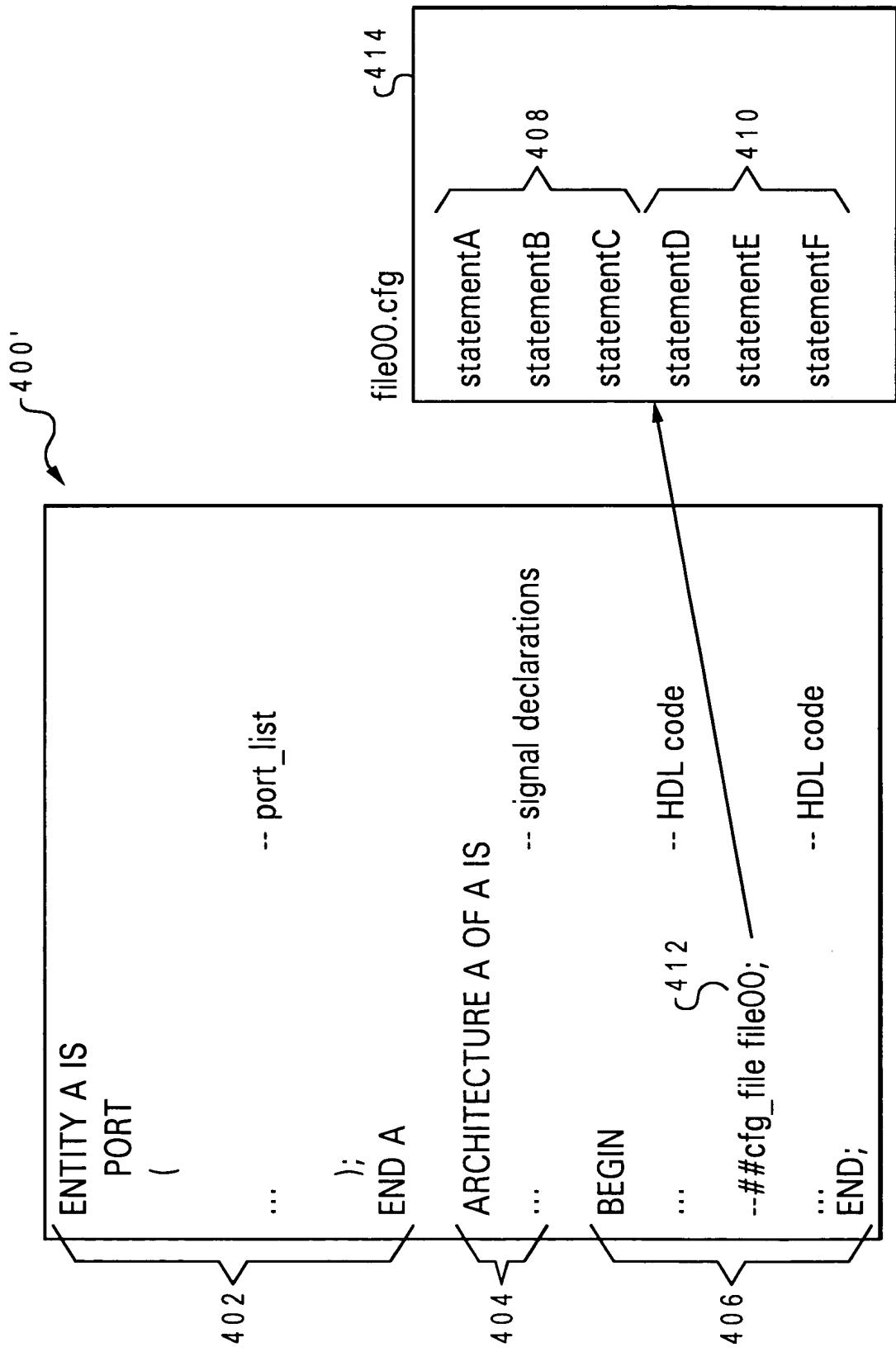
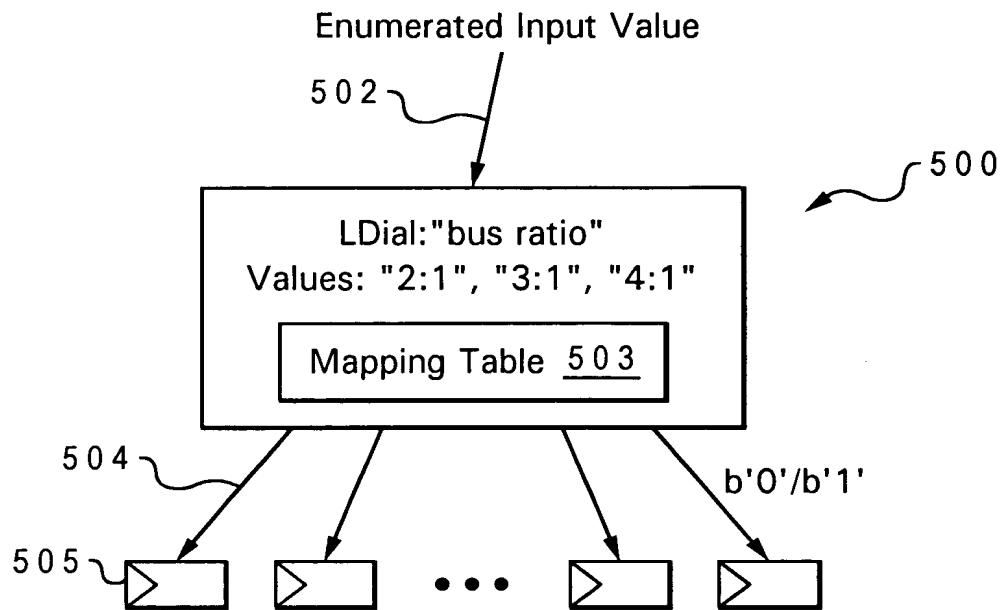
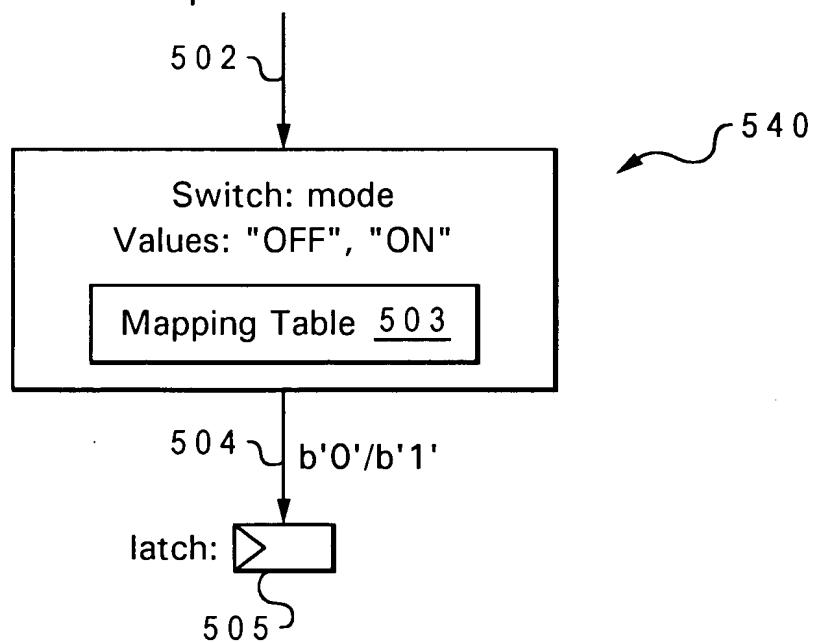


Fig. 4B



*Fig. 5A*

Enumerated Input Value: "ON" or "OFF"



*Fig. 5D*

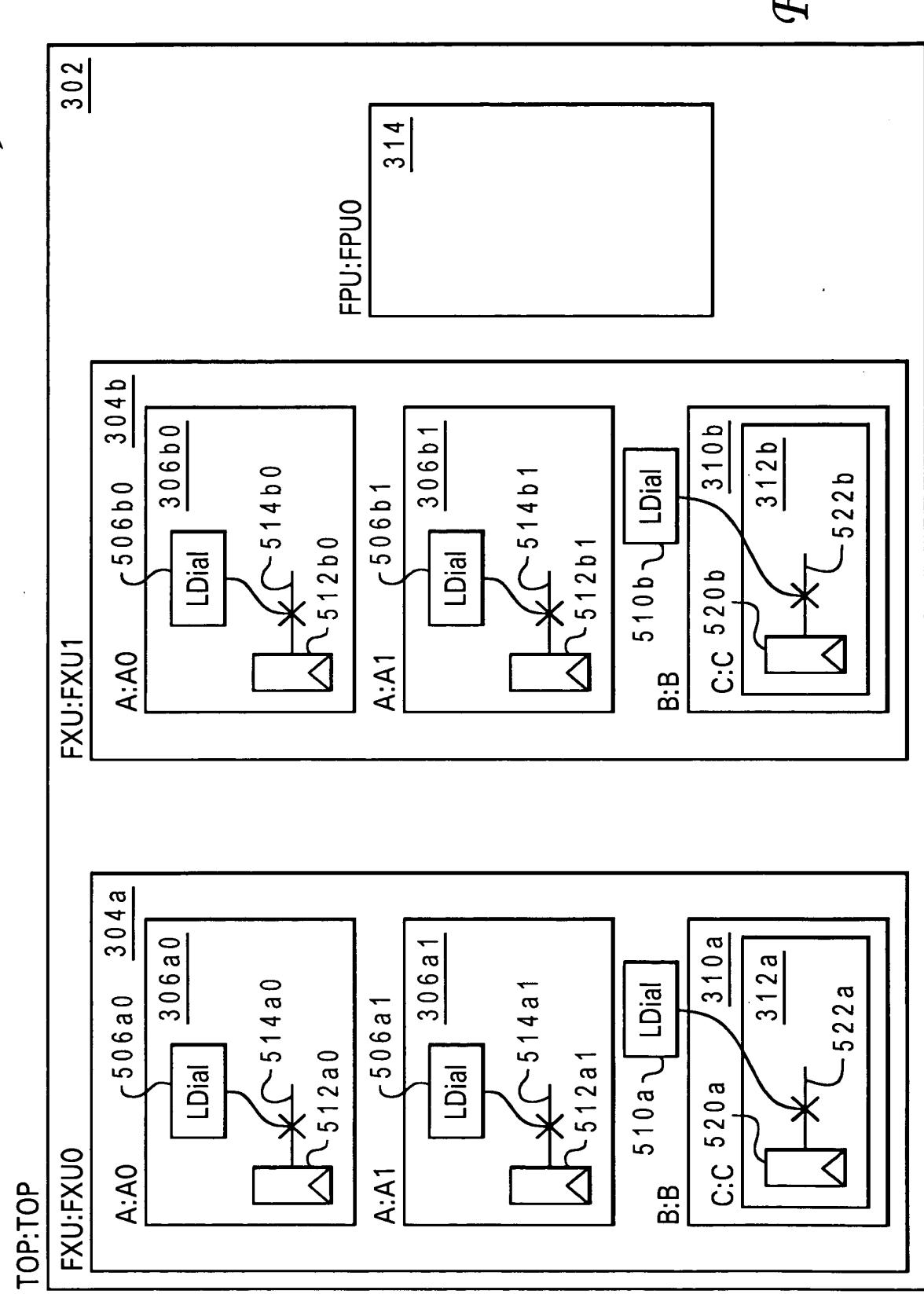
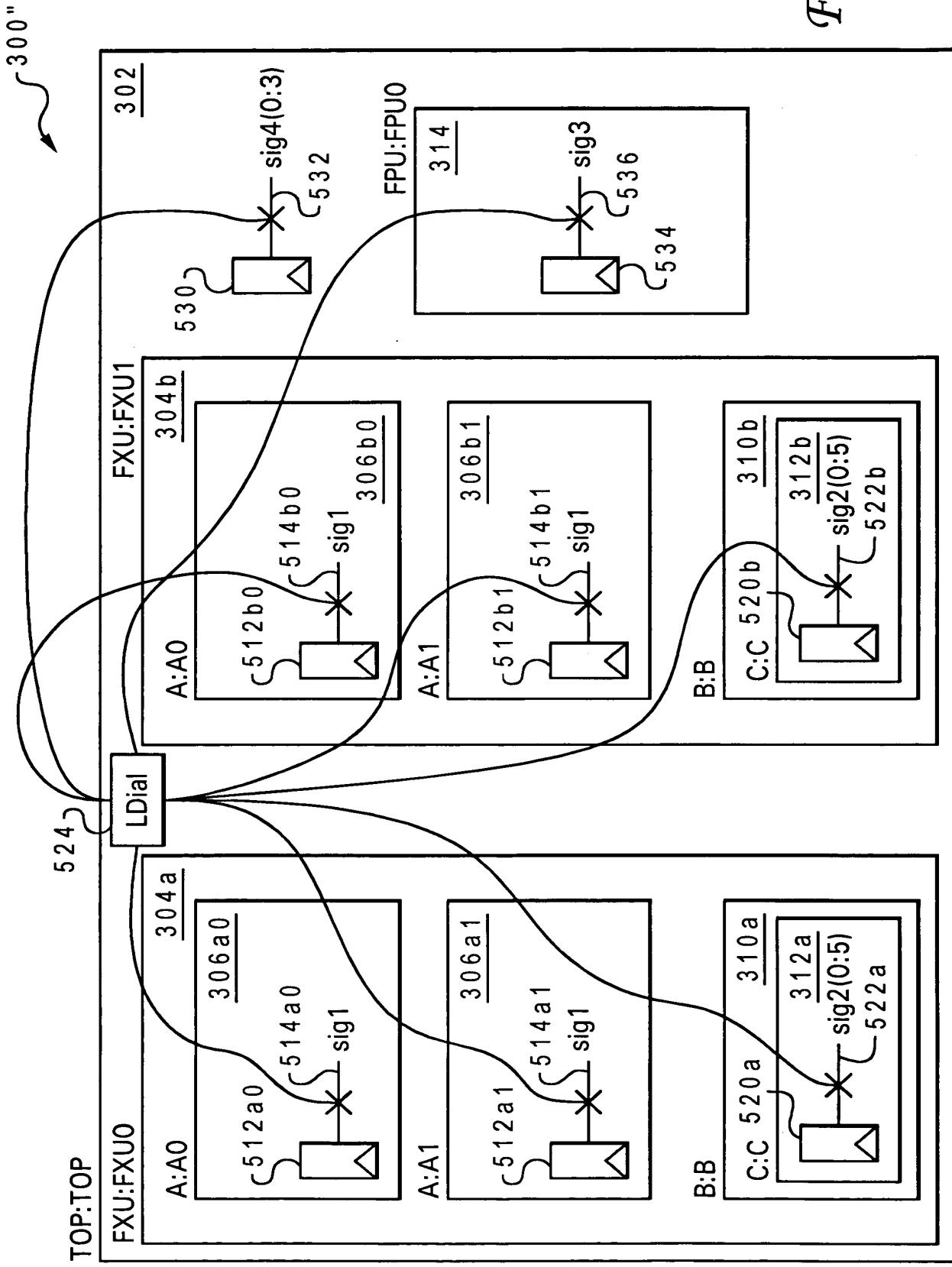
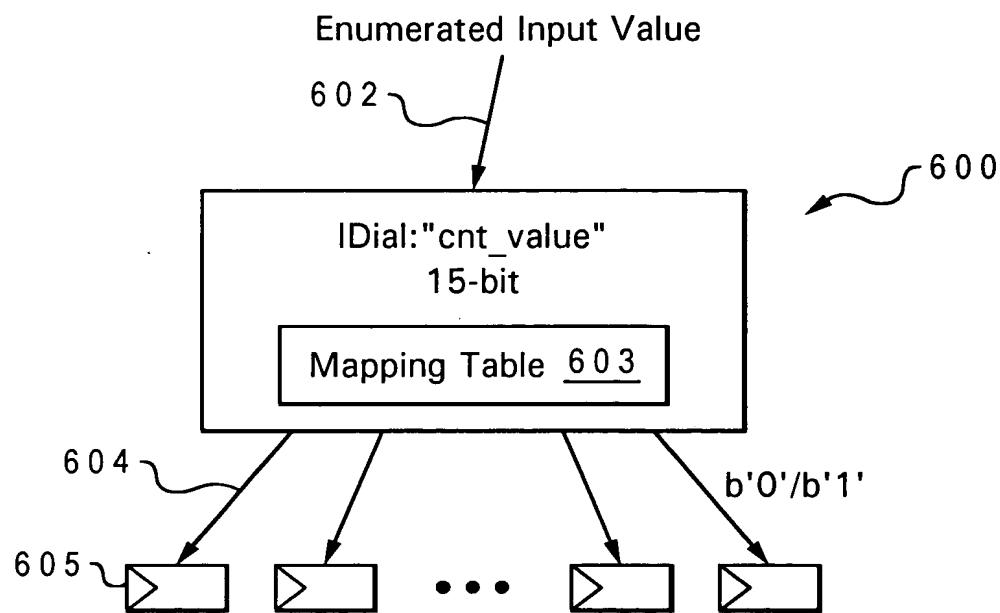
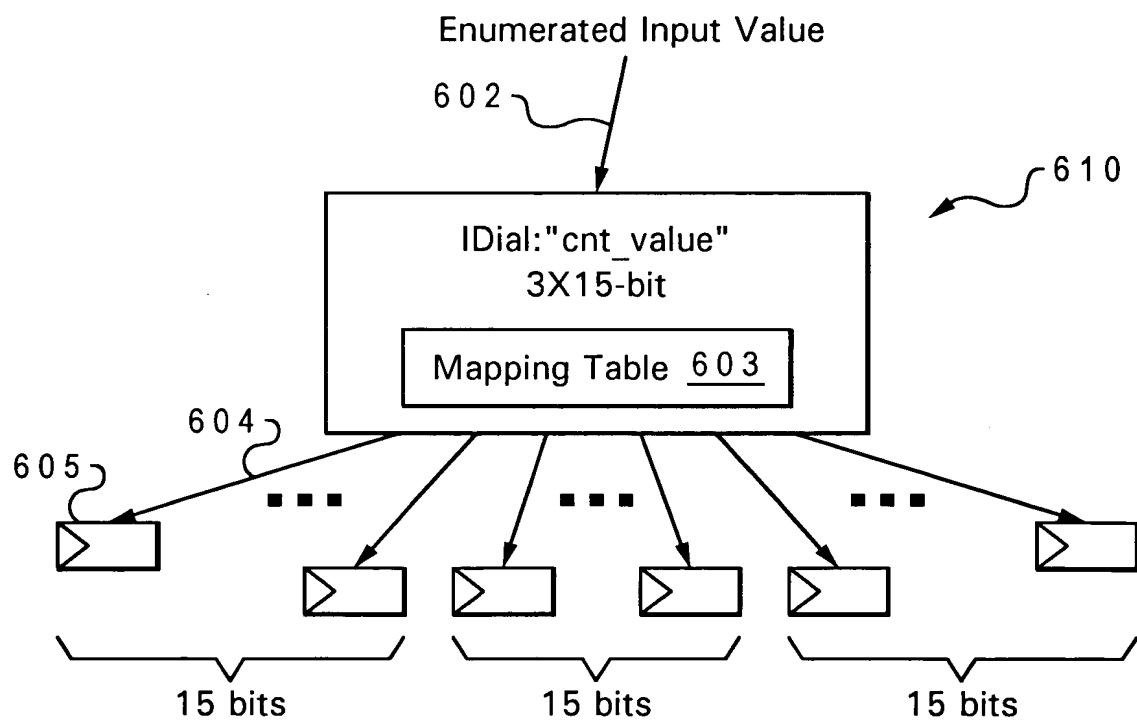


Fig. 5C





*Fig. 6A*



*Fig. 6B*

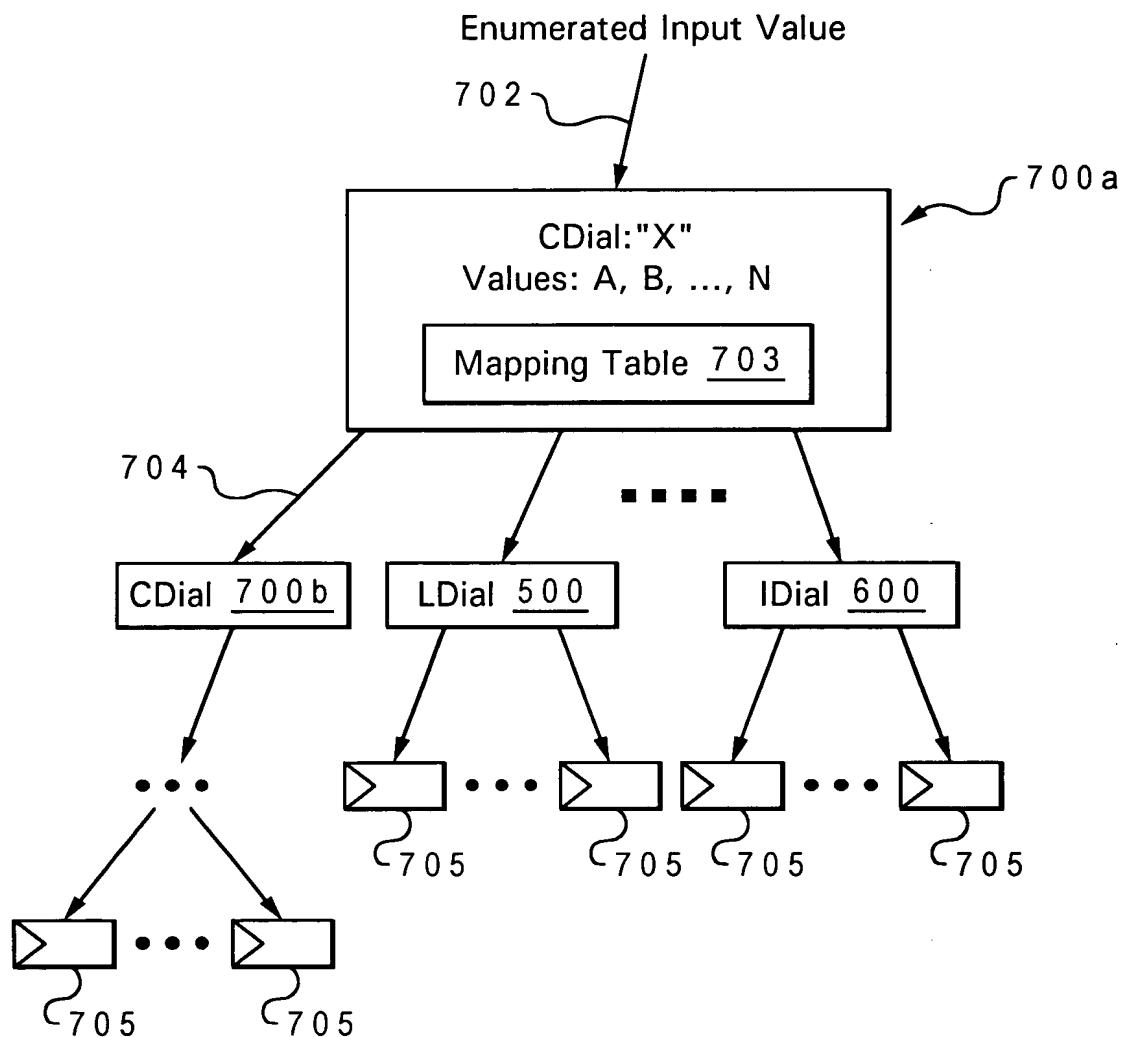
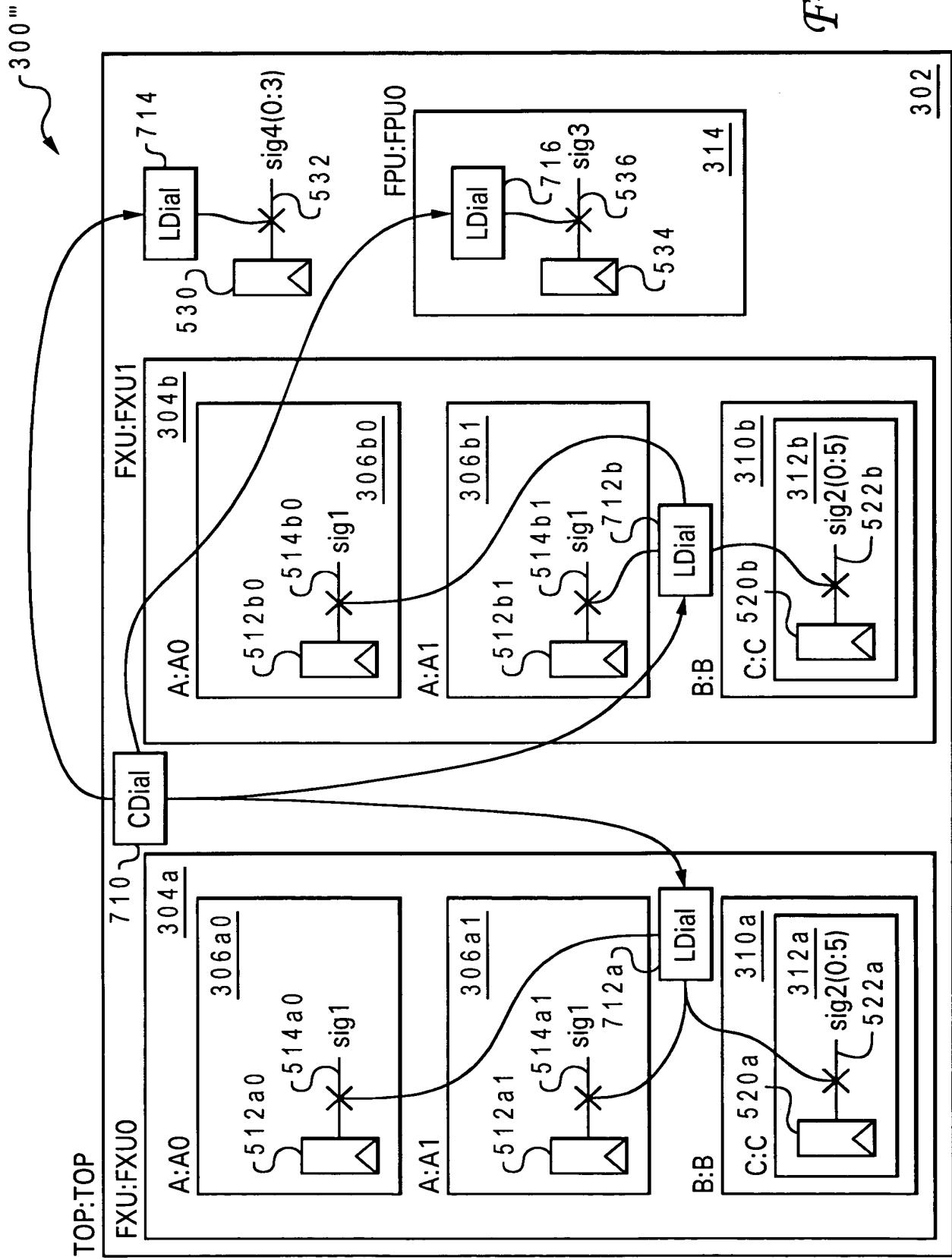
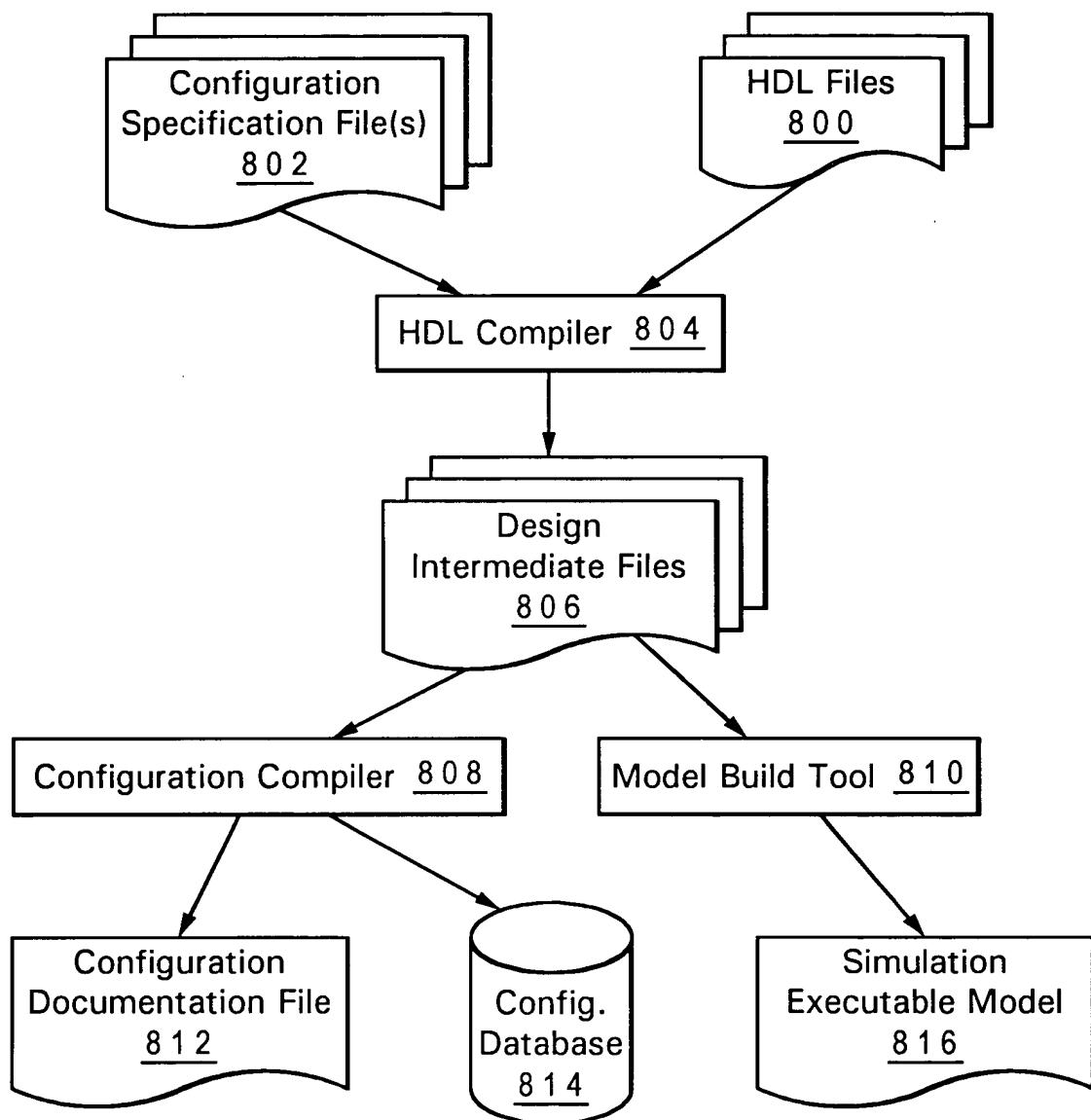


Fig. 7A

Fig. 7B





*Fig. 8*

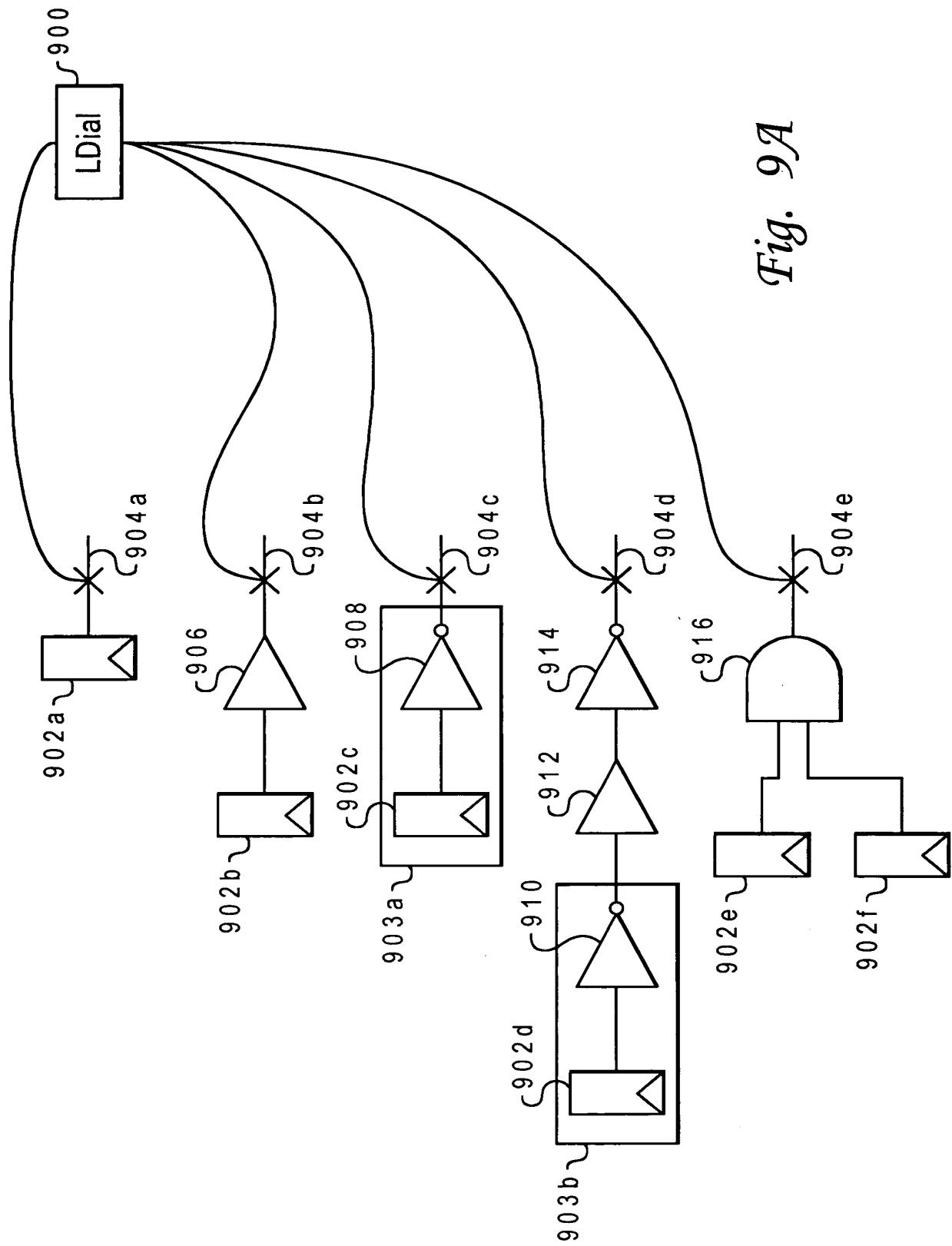


Fig. 9A

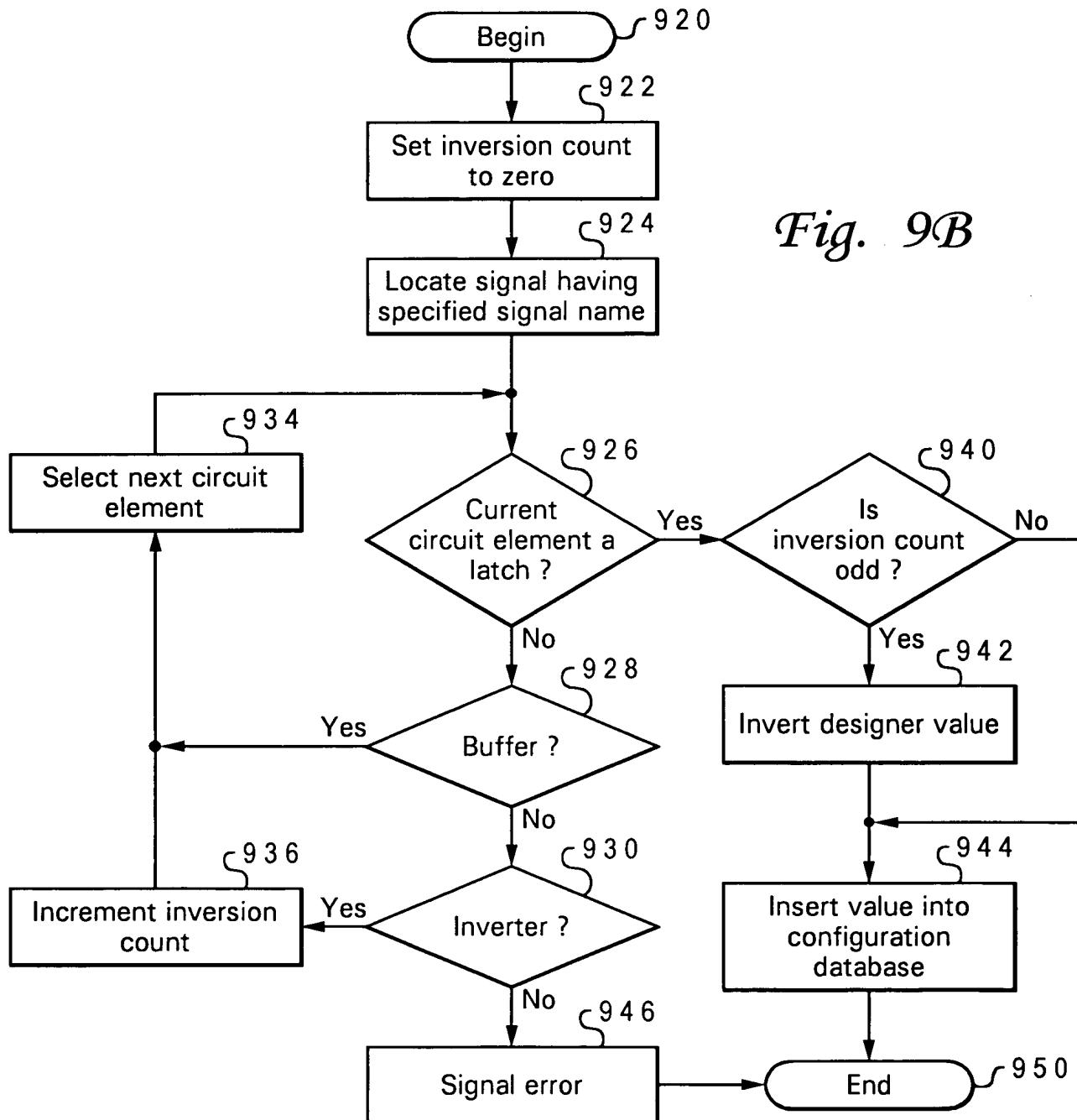
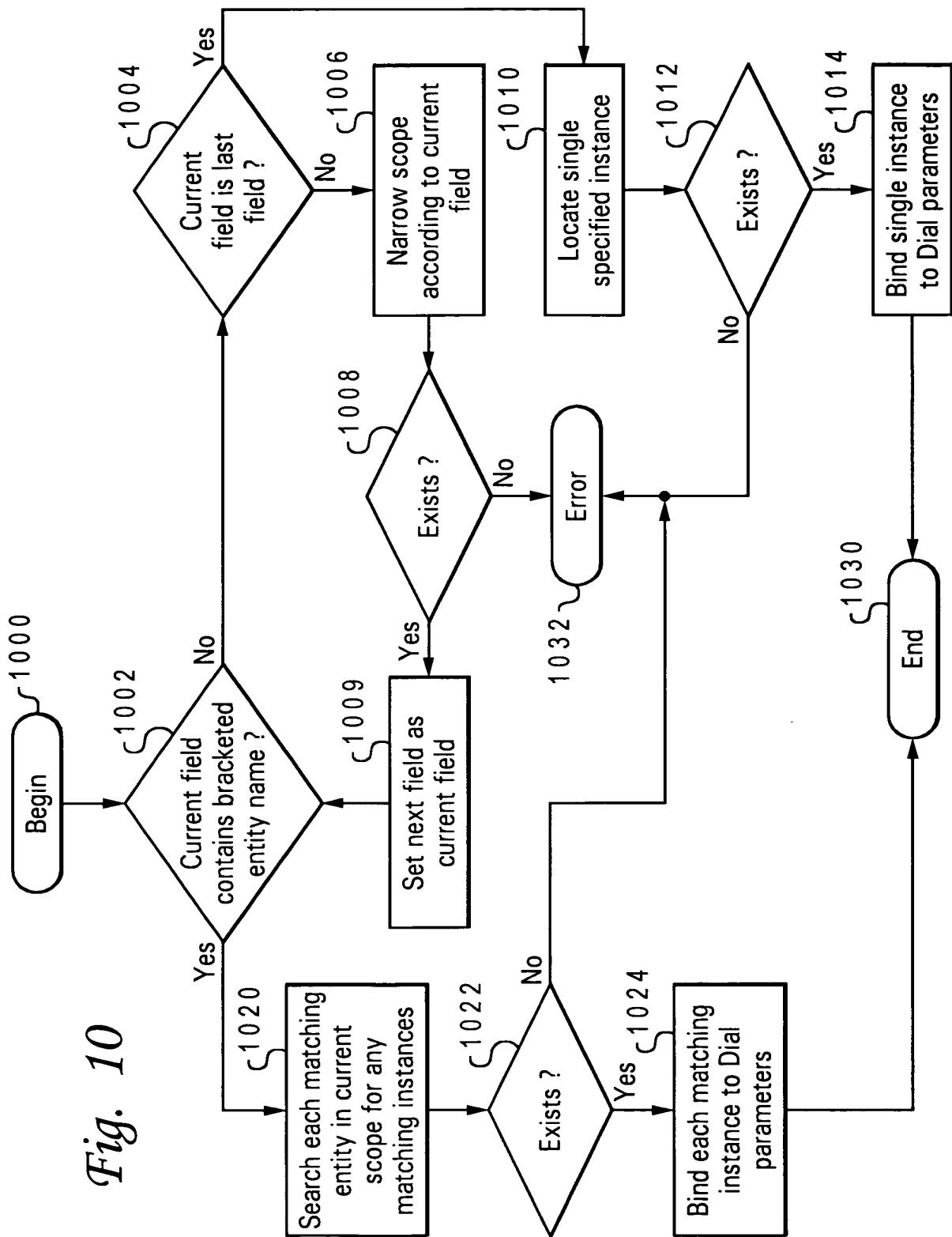


Fig. 9B



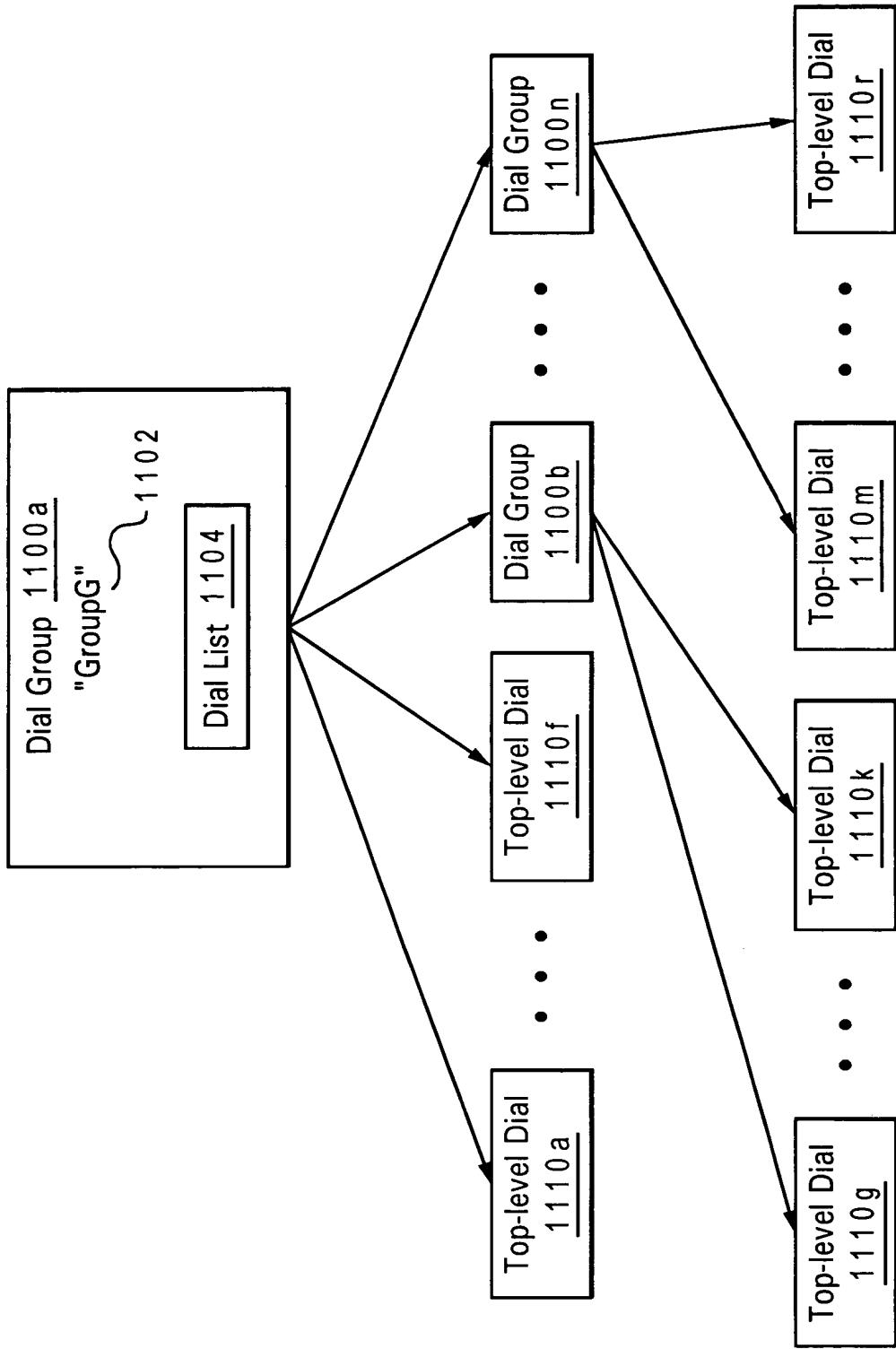


Fig. 11A

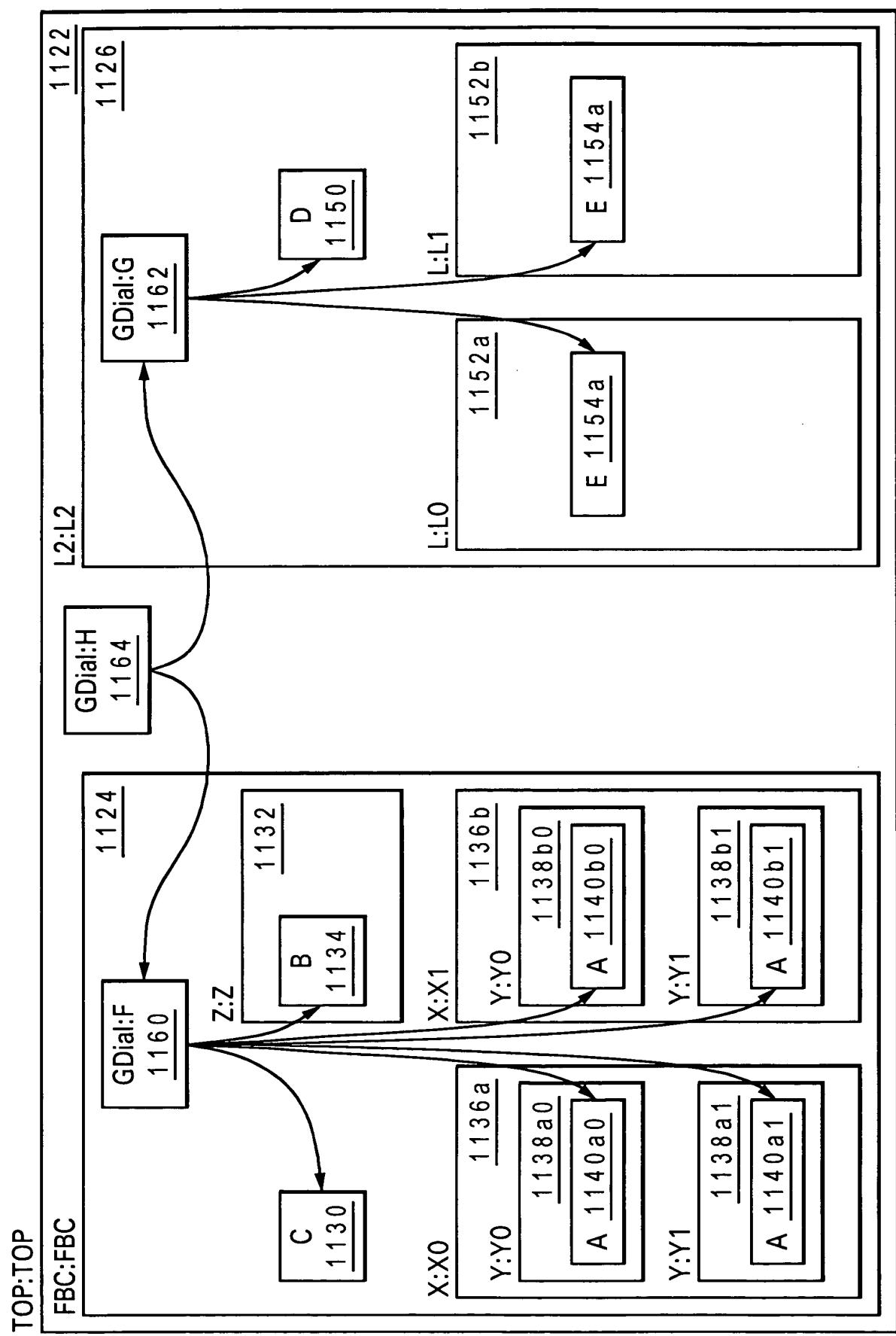
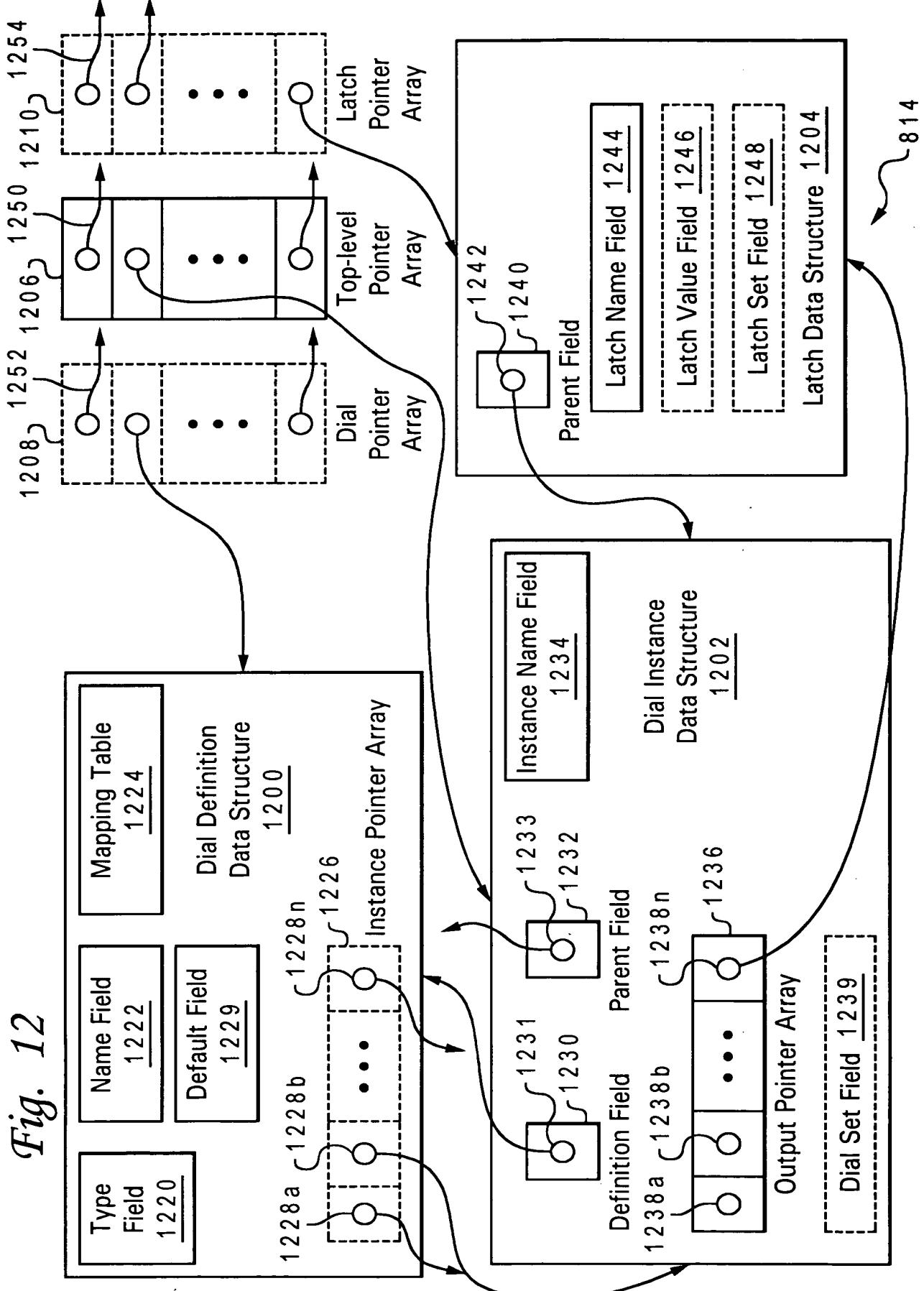


Fig. 11B

Fig. 12



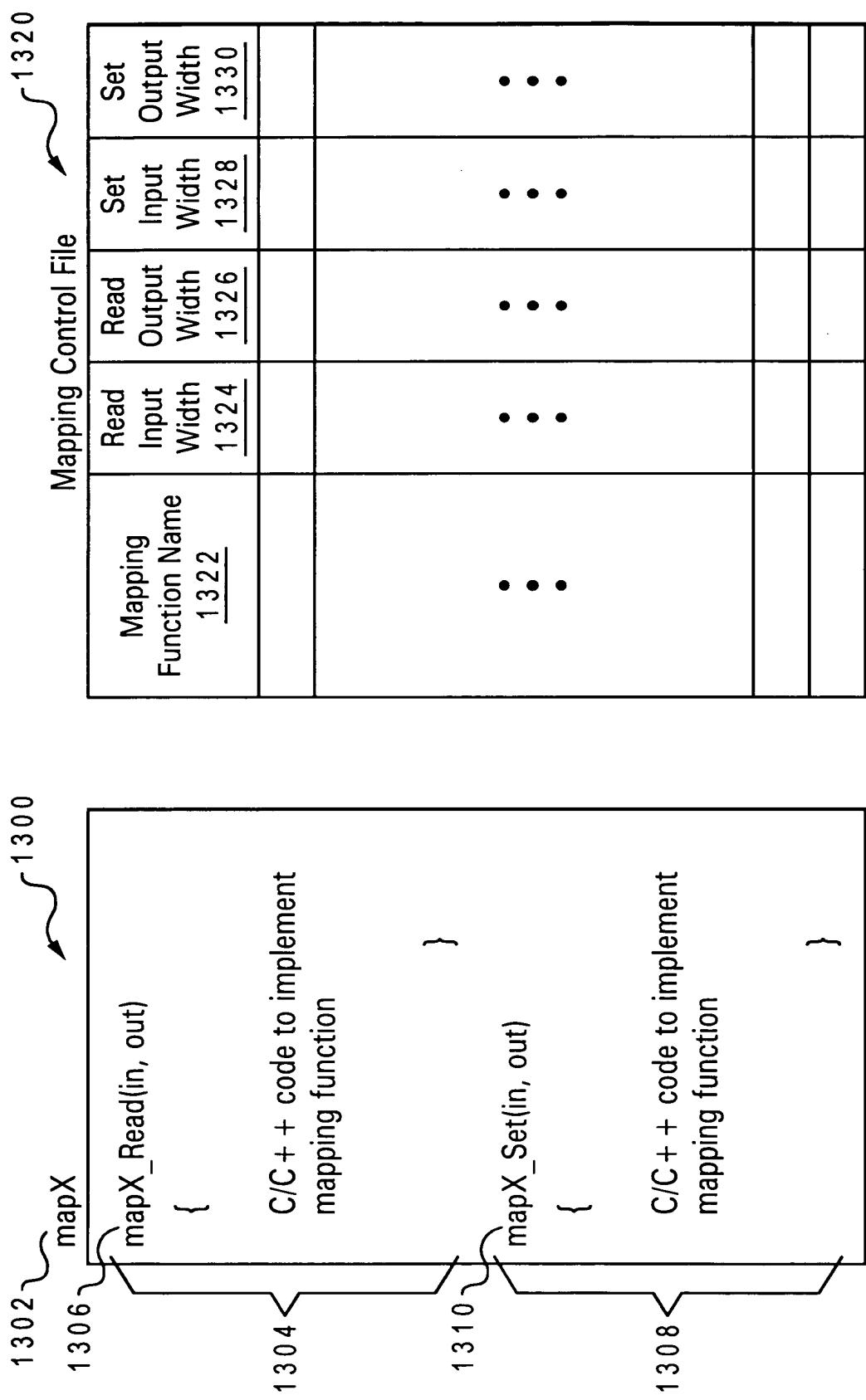
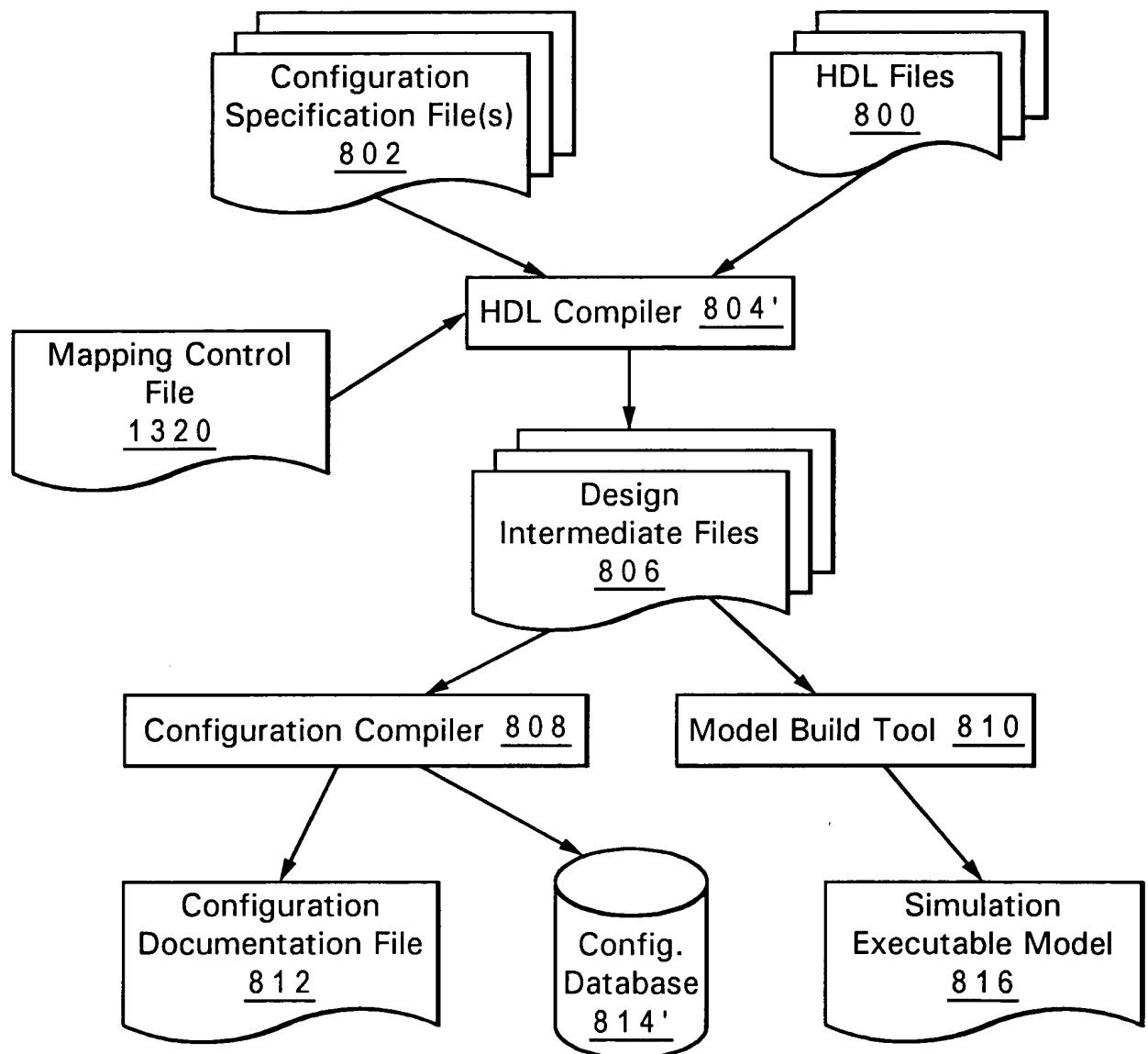


Fig. 13A

Fig. 13B



*Fig. 14*

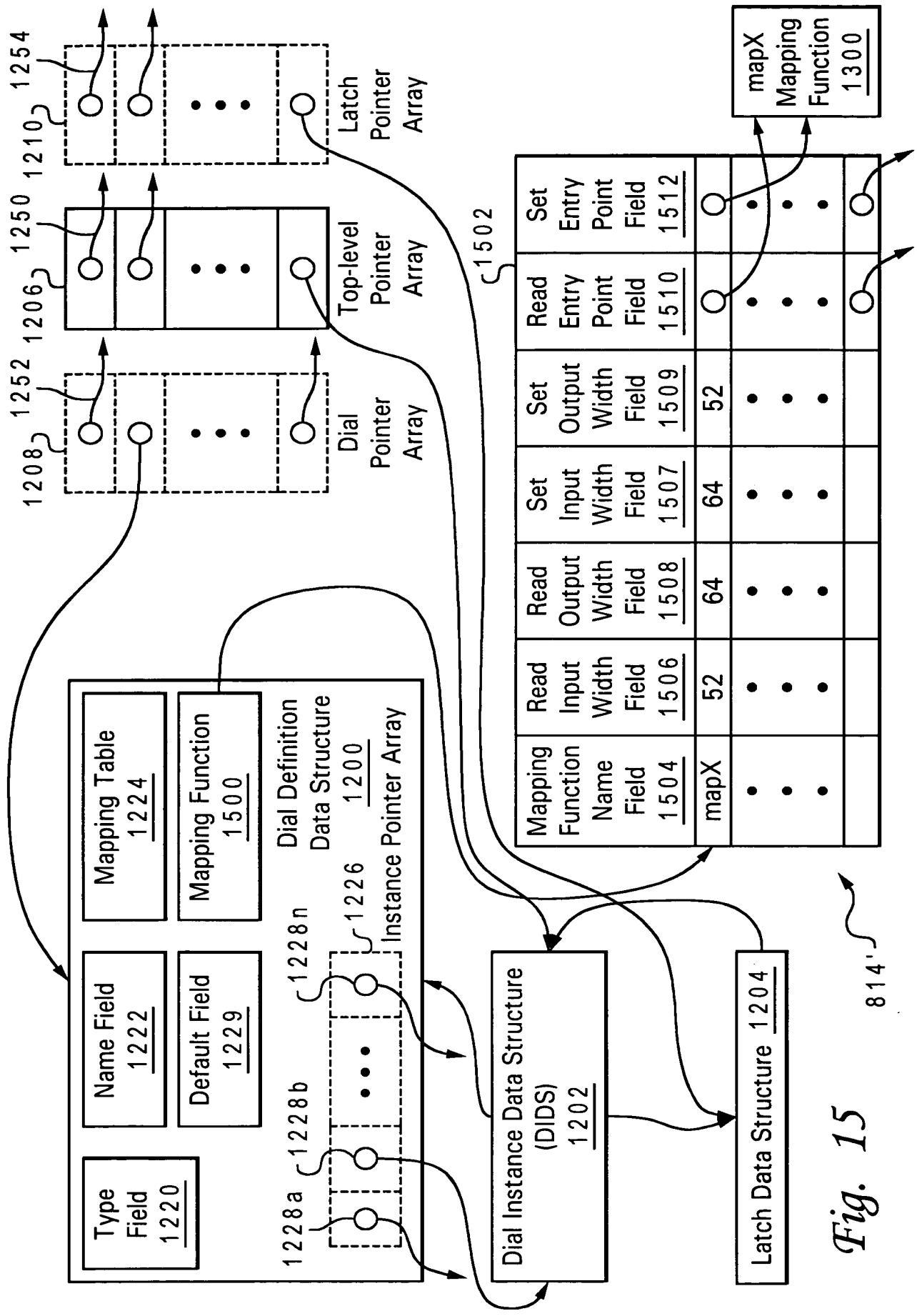


Fig. 15 814 ↗

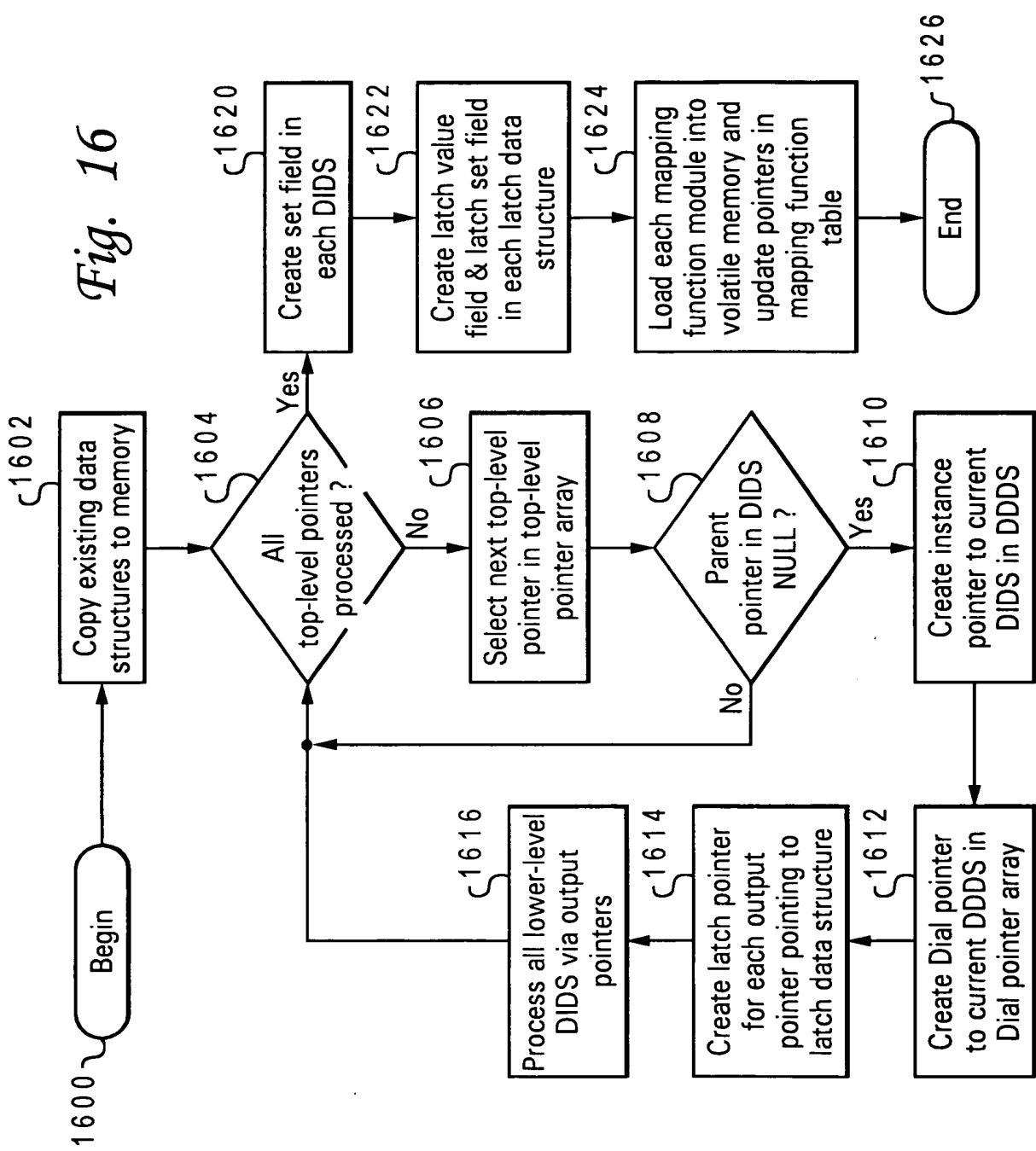
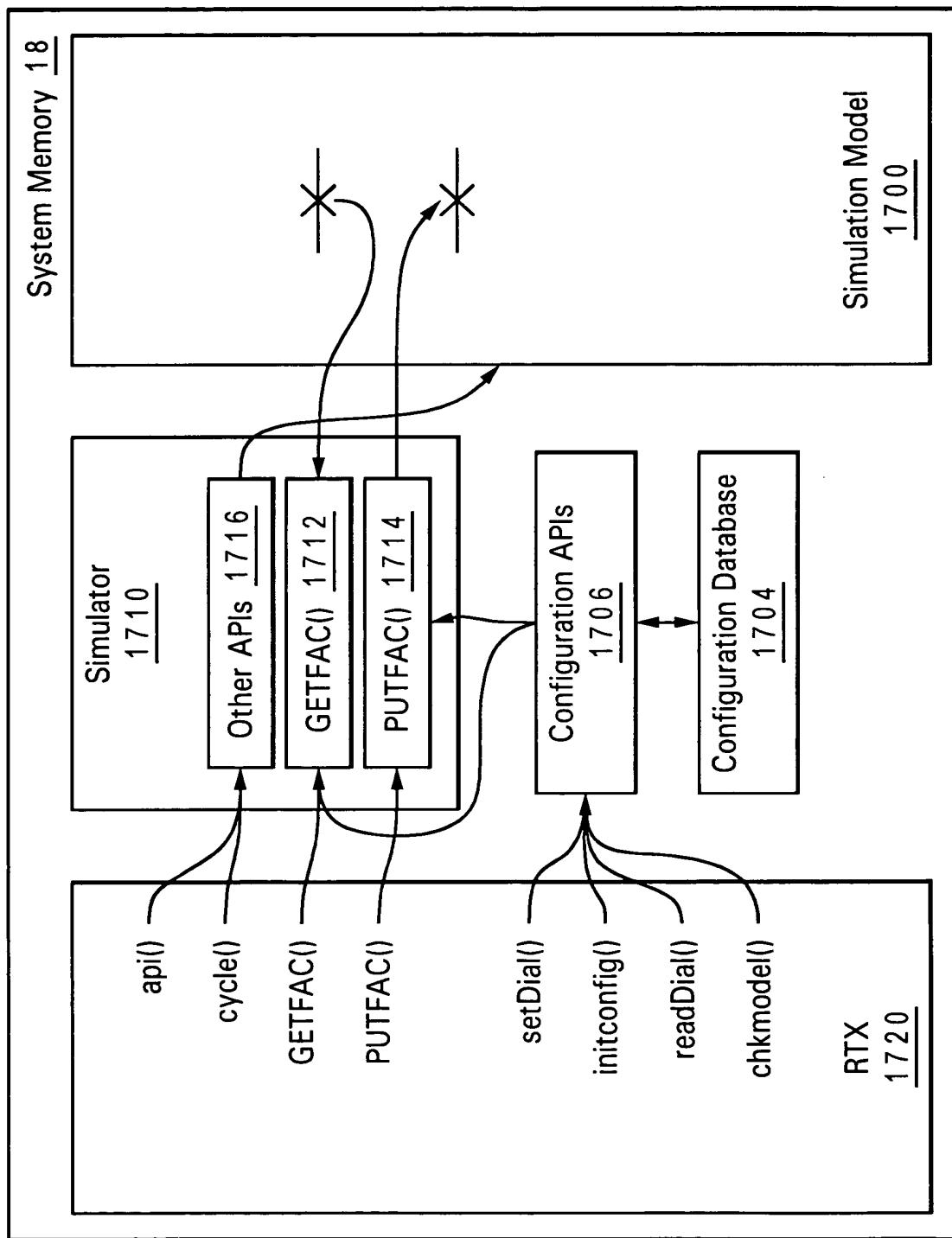


Fig. 17



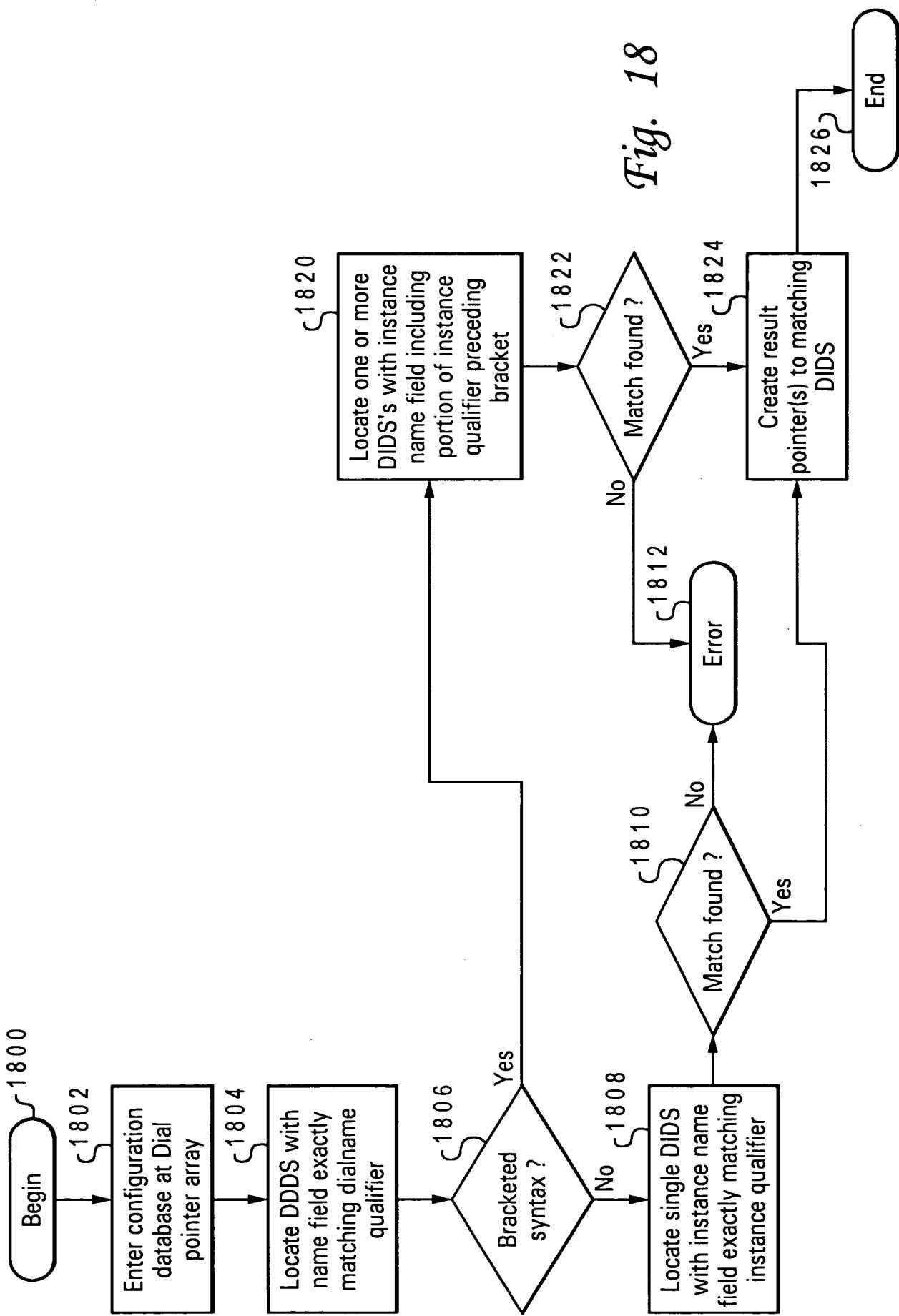
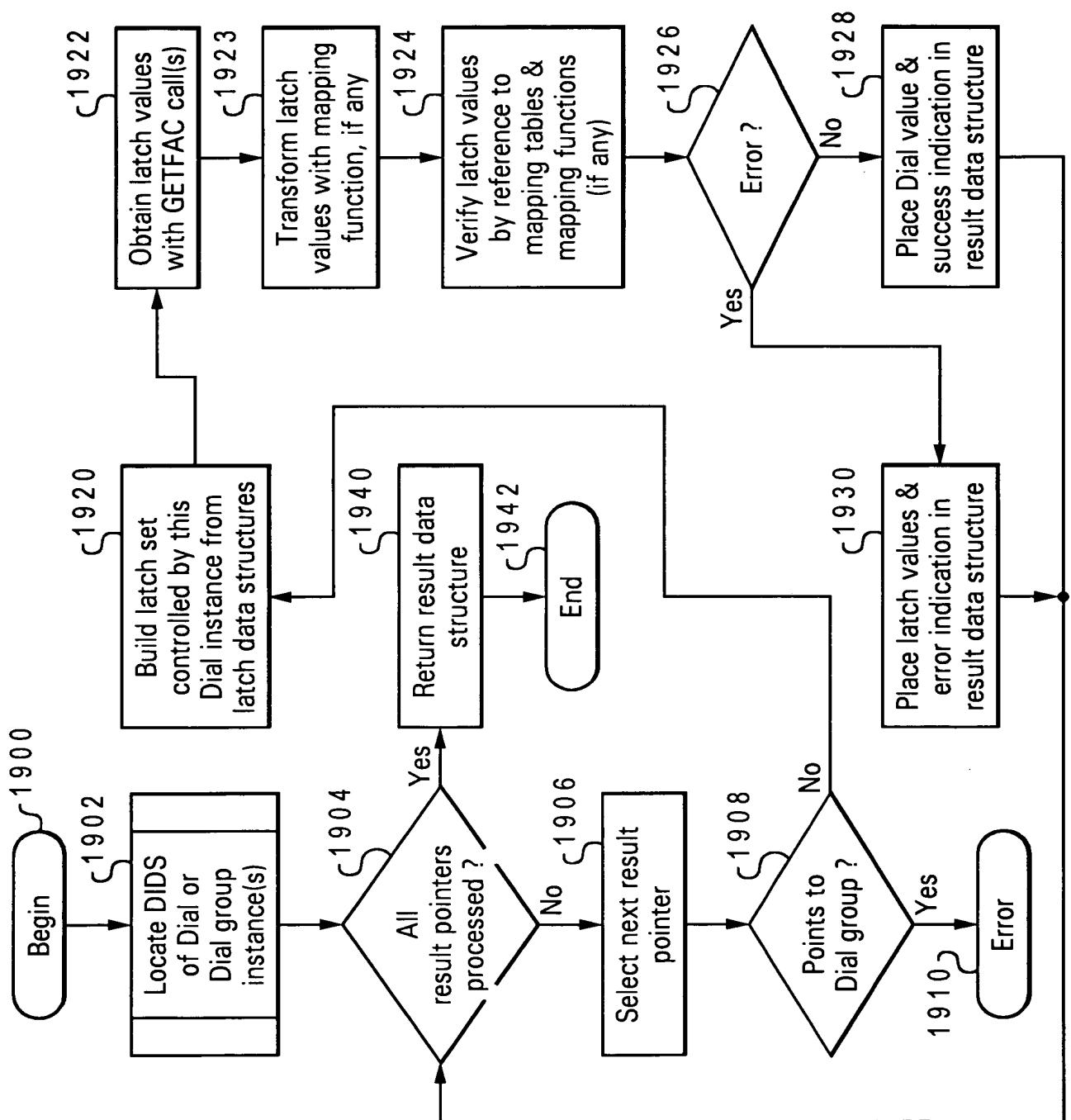


Fig. 19A



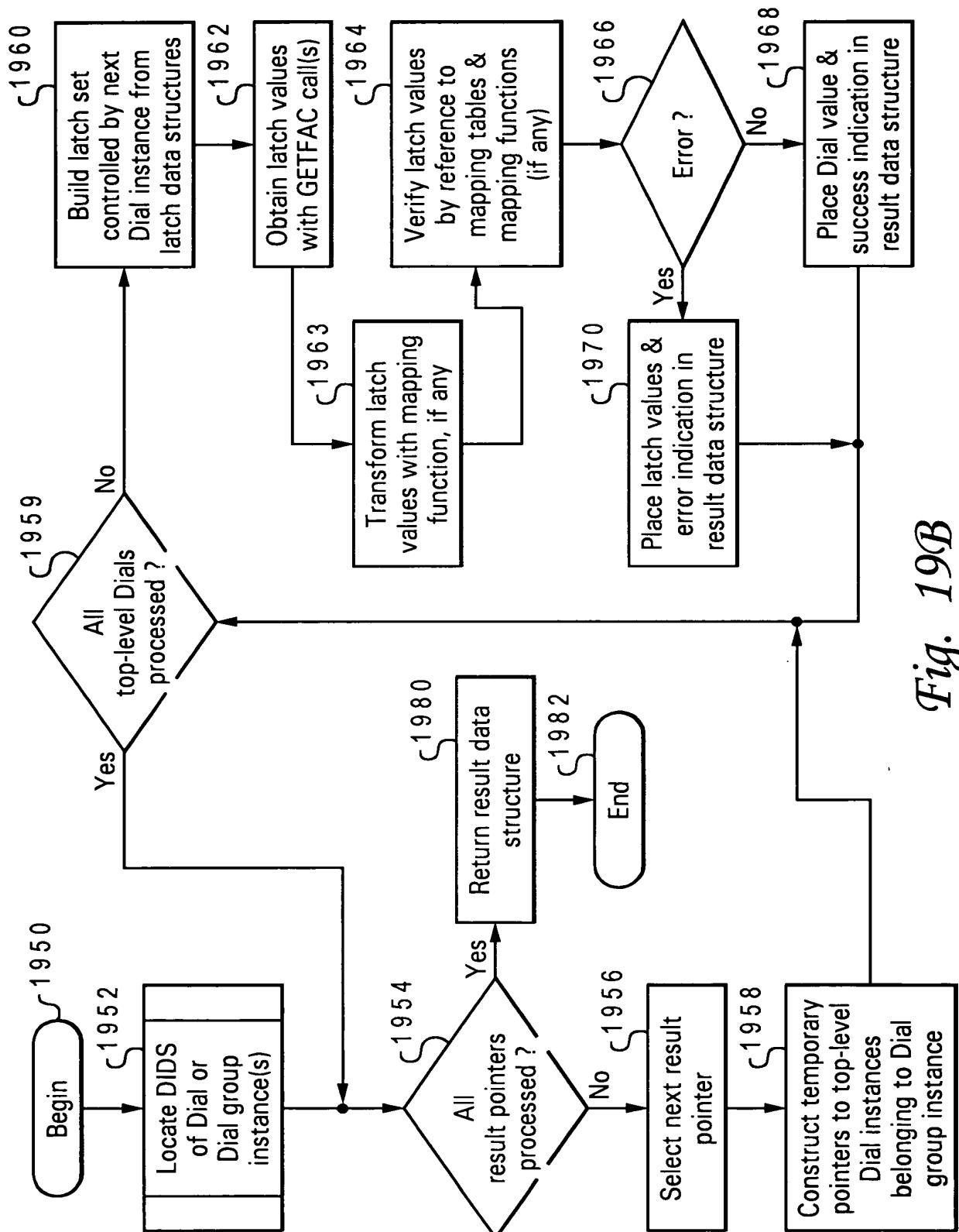


Fig. 19B

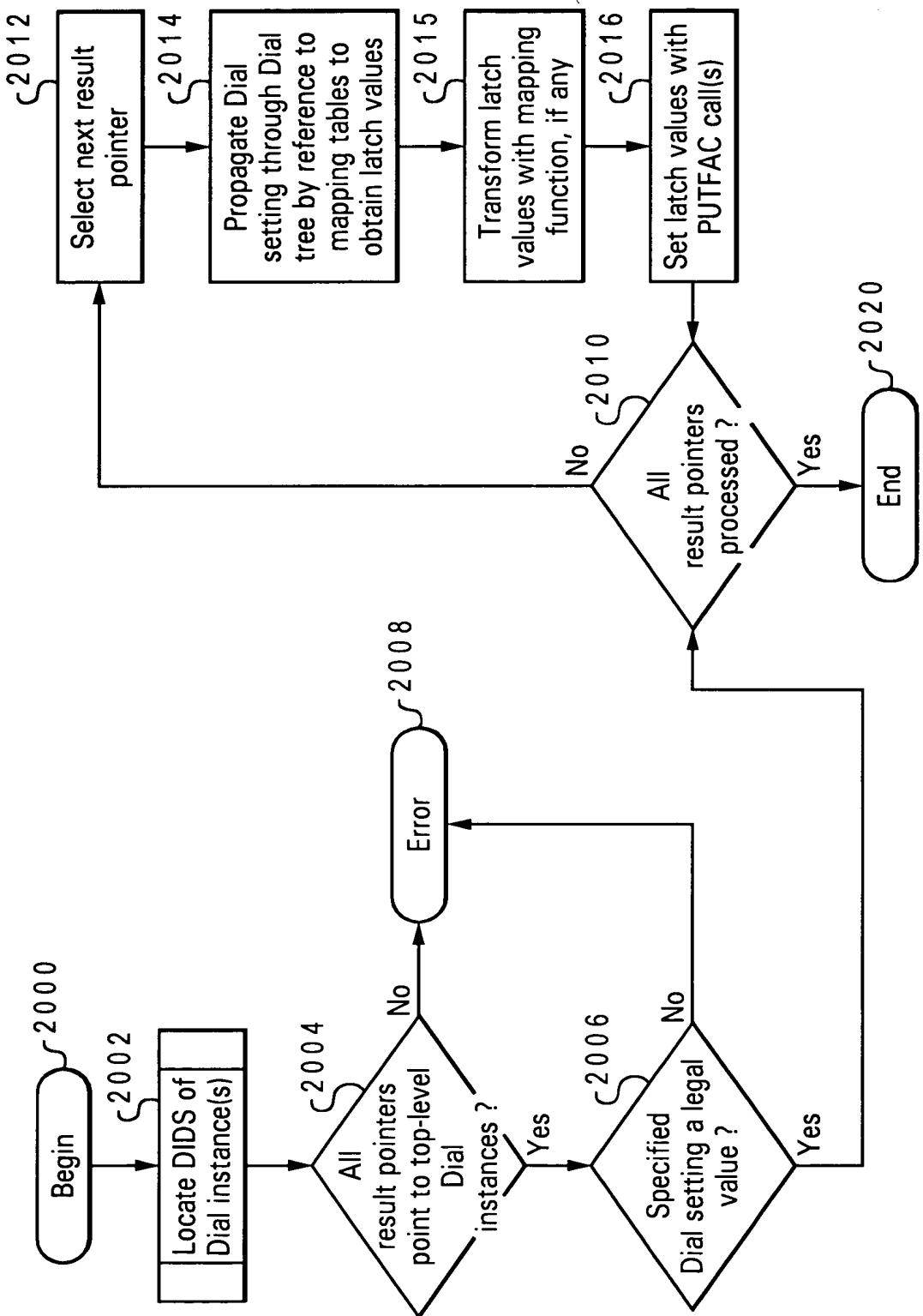


Fig. 20A

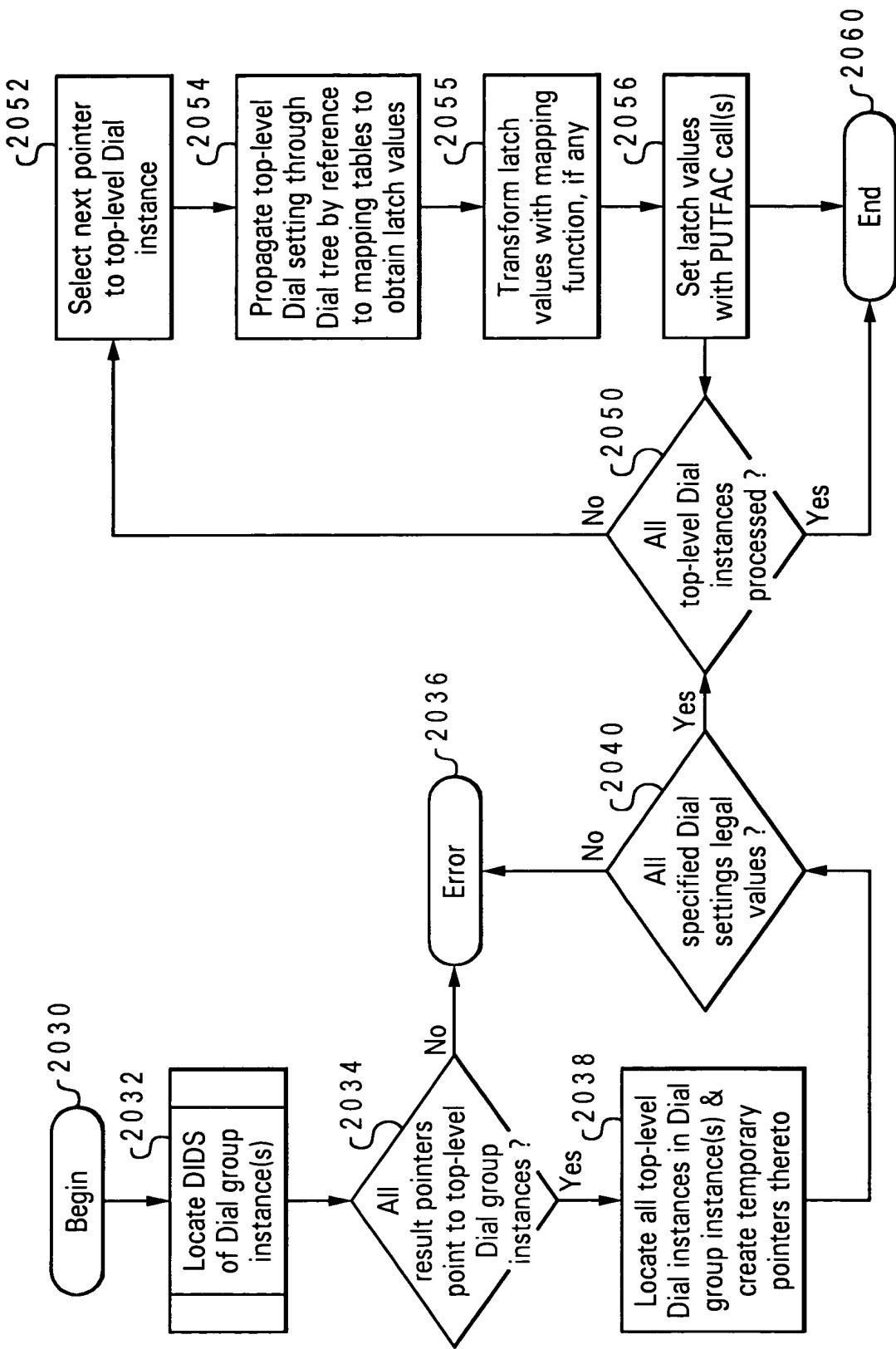
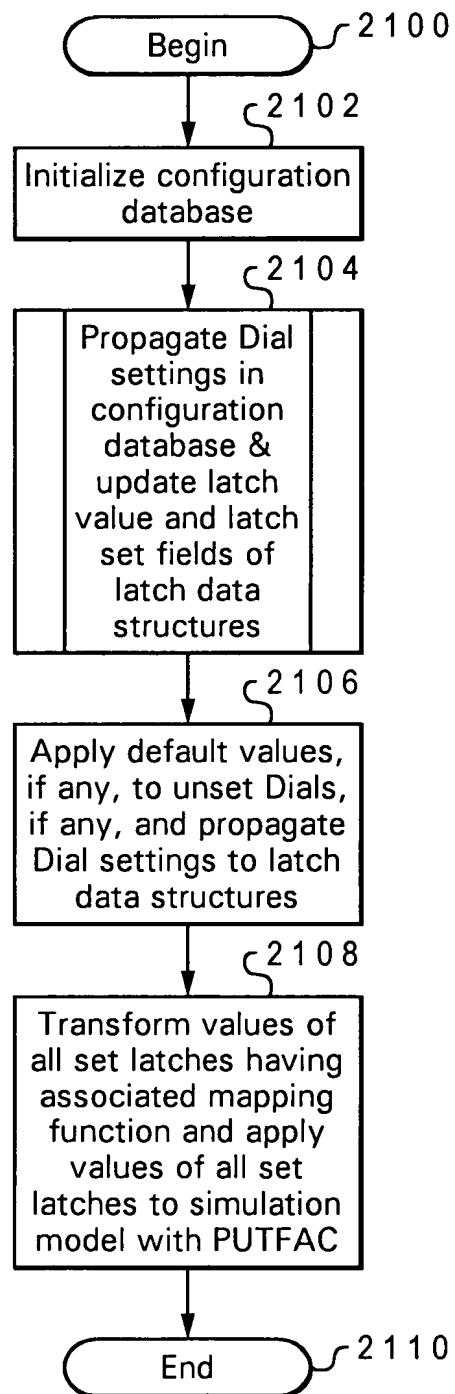


Fig. 20B



*Fig. 21*